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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,405	NIE, XIAONING	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005 and 14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04 August 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 4-12 have been considered. Claim 1 is amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 04 August 2005; Amendment as received on 24 August 2005; and RCE as received on 14 October 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki, U.S. Patent Number 6,499,096 (herein referred to as Suzuki) in view of Kahle et al., U.S. Patent Number 5,913,925 (herein referred to as Kahle) and in further view of Heishi et al., U.S. Patent Number 6,324,639 (herein referred to as Heishi).

5. Referring to claim 1, Suzuki has taught a data-processing device for processing in parallel a plurality of processes, comprising:

a. A multiplicity of bundles with a plurality of instructions of a process, the instructions of a bundle being executable in parallel (Suzuki column 2, lines 14-29);

b. A branching control unit connected to and addressing said program memory a register for storing flags and data which are switched in dependence on a process

being executed (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11);

c. A program flow control unit connected to said branching control unit (Suzuki column 6, lines 29-44 and 52-67 and Figure 3), said program flow control unit controlling a fetching of bundles to be processed in parallel from said program memory, controlling said branching control unit, and controlling an output of instructions to be processed in parallel in dependence on information contained in the instructions and included in a compiling time of the program (Suzuki column 6, lines 29-44 and 52-67 and Figure 3);

d. A number N of instruction buffers being connected in parallel downstream of said program memory for storing instructions read out from said program memory (Suzuki column 4, line 56 to column 5, line 6; column 12, lines 7-13; column 12, line 36 to column 13, line 5; Figure 3; Figure 9; and Figure 11), an instruction bundle being read into one of said instruction buffers and a second instruction bundle associated with a different process being read into another one of said instruction buffers(Suzuki column 4, line 56 to column 5, line 6; column 12, lines 7-13; column 12, line 36 to column 13, line 5; Figure 3; Figure 9; and Figure 11); and

e. An instruction output selector being connected to and controlled by said process flow control unit causing said instruction output selector to read out instructions from said instruction buffers and output N instructions in parallel (Suzuki column

7, line 62 to column 8, line 24; column 12, line 36 to column 13, line 6; Figure 3; and Figure 11).

6. Suzuki has not explicitly taught said instruction output selector having a multiplexer logic and selecting in a first case one of either one instruction from a first instruction buffer and one instruction from a second instruction buffer and in a second case two instructions from one of said first and second instruction buffers. However, Suzuki has taught selecting output from multiple buffers (Suzuki column 7, line 62 to column 8, line 24; column 12, line 36 to column 13, line 6; Figure 3; and Figure 11). Heishi has explicitly taught said instruction output selector having a multiplexer logic and selecting in a first case one of either one instruction from a first instruction buffer and one instruction from a second instruction buffer and in a second case two instructions from one of said first and second instruction buffers (Heishi column 13, lines 1-7 and 19-53; column 14, lines 1-62; Figure 8; Figure 9; and Figure 10). A person of ordinary skill in the art at the time the invention was made would have recognized that the selector of Heishi maximizes the number of instructions in parallel without specialized hardware (Heishi column 4, lines 45-54), thereby decreasing size and increasing efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the buffer selector of Heishi in the device of Suzuki to reduce chip size and increase processing efficiency.

7. In addition, Suzuki has not taught a program memory having stored therein at least one compiled program with a multiplicity N of independent processes, the compiled program including information on parallelism. Kahle has taught a program memory having stored therein at least one compiled program with a multiplicity N of independent processes, the compiled

program including information on parallelism (Kahle column 2, lines 64 to column 3, line 2; column 4, lines 33-46; and Figure 1A). A person of ordinary skill in the art at the time the invention was made that the multiscalar device of Kahle utilizes more of the hardware resources and diminishes the effects of mispredicted branches and data dependencies between tasks (Kahle column 3, lines 59-66), thereby improving processor performance. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiscalar device of Kahle in the device of Suzuki to improve processor performance.

8. Referring to claim 4, Suzuki has taught which comprises N instruction decoders for decoding the instructions being output (Suzuki column 4, line 56 to column 5, line 6; column 12, lines 7-13; column 12, line 36 to column 13, line 5; Figure 3; Figure 9; and Figure 11).

9. Referring to claim 5, Suzuki has taught which comprises at least two instruction-execution units for outputting the N decoded instructions (Suzuki column 4, line 56 to column 5, line 6; column 12, lines 7-13; column 12, line 36 to column 13, line 5; Figure 3; Figure 9; and Figure 11).

10. Referring to claim 6, Suzuki has not taught which comprises a data memory and at least two buses connecting said N instruction-execution units to said data memory. Kahle has taught which comprises a data memory and at least two buses connecting said N instruction-execution units to said data memory (Kahle column 10, lines 26-33 and Figure 4). A person of ordinary skill in the art at the time the invention was made that the multiscalar device of Kahle utilizes more of the hardware resources and diminishes the effects of mispredicted branches and data dependencies between tasks (Kahle column 3, lines 59-66), thereby improving processor

performance. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiscalar device of Kahle in the device of Suzuki to improve processor performance.

11. Referring to claim 7, Suzuki has taught which comprises a plurality of instruction-execution units connected to said program flow control unit and configured to execute the instructions of one or more bundles in parallel (Suzuki column 4, line 56 to column 5, line 6; column 12, lines 7-13; column 12, line 36 to column 13, line 5; Figure 3; Figure 9; and Figure 11).

12. Referring to claim 8, Suzuki has taught wherein said branching control unit is configured to output an address pointer for addressing a bundle (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11).

13. Referring to claims 9 and 11, Suzuki has taught wherein the branching control unit comprises:

a. A first multiplexer and a second multiplexer (Applicant's claim 9) (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11);

b. An adder (Applicant's claim 9) (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11);

c. Wherein said program flow control unit feeds a number of instructions in a bundle to said adder and said adder adds an address pointer and the number of instructions (Applicant's claim 9) (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11);

d. Wherein said program flow control unit feeds addresses for program jumps or function calls and a process number to said first multiplexer (Applicant's claim 9) (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11);

e. Said first multiplexer writing either the output signal of said adder or the addresses for program jumps or function calls into said program counter assigned to the active process (Applicant's claim 9) (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11); and

f. A content of said program counter assigned to the currently active process is output as a new address pointer via said, second multiplexer which is controlled using the process number supplied (Applicant's claim 9) (Suzuki column 6, lines 29-44 and 52-67; column 12, line 36 to column 13, line 5; Figure 3; and Figure 11).

g. Wherein said program flow control unit is configured to receive via a subbus of an output bus of said program memory at least one of the following:

i. At least one bit for indicating the parallel execution of instructions (Applicant's claim 10) (Suzuki column 2, lines 14-29). In regards to Suzuki, the at least one bit is inherent for the instruction to be recognized as a VLIW instruction.

ii. At least one bit for indicating the length of the following instruction bundle (Applicant's claim 10) (Suzuki column 4, line 56 to column 5, line 6; column 12, lines 7-13; column 12, line 36 to column 13, line 5; Figure

3; Figure 9; and Figure 11). In regards to Suzuki, the at least one bit is inherent for the instruction to recognize where it ends, since the instructions contains multiple sub-instructions.

iii. The indication of one or more NOPs in the instruction bundles (Applicant's claim 10) (Suzuki column 3, lines 49-52).

14. Suzuki has not taught

a. N program counters (Applicant's claim 9);

b. A priority of the processes of the instructions (Applicant's claim 10);

c. Wherein a process is called with a run instruction assigning a process number, a priority and a memory address of a starting point of the process in the program memory (Applicant's claim 11).

15. Kahle has taught

a. N program counters (Applicant's claim 9) (Kahle column 10, lines 26-33 and Figure 4);

b. A priority of the processes of the instructions (Applicant's claim 10) (Kahle column 10, line 52 to column 11, line 29)

c. Wherein a process is called with a run instruction assigning a process number, a priority and a memory address of a starting point of the process in the program memory (Applicant's claim 11) (Kahle column 10, line 52 to column 11, line 29).

16. The program counters are inherent, since the position of the instruction for each thread in the individual instruction caches must be known. Program counters indicate which instruction is to executed next. A person of ordinary skill in the art at the time the invention was made that the

multiscalar device of Kahle utilizes more of the hardware resources and diminishes the effects of mispredicted branches and data dependencies between tasks (Kahle column 3, lines 59-66), thereby improving processor performance. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiscalar device of Kahle in the device of Suzuki to improve processor performance.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki, U.S. Patent Number 6,499,096 (herein referred to as Suzuki) in view of Kahle et al., U.S. Patent Number 5,913,925 (herein referred to as Kahle) and in further view of Heishi et al., U.S. Patent Number 6,324,639 (herein referred to as Heishi), as applied to claim 1 above, and further in view of Allen, Jr. et al., U.S. Patent No. 6,404,752 (herein referred to as Allen). Suzuki in view of Kahle has not explicitly taught wherein said data processing device is a network processor for processing layer 1 to 7 of protocol stacks in applications including LAN, ATM switches, IP routers, and frame relays based on a system selected from the group consisting of DSL, Ethernet, and cable modems. Allen has taught the use of general-purpose microprocessors as network processors to provide a cost-effective solution to processing protocol stack layers for IDSN, cable and DSL modems that provides high throughput and speeds (Allen column 1, lines 44-49 and column 2, line 38 to column 3, line 23). One of ordinary skill in the art would have recognized that a primary goal in microprocessor design is to lower costs while maintaining a high level of performance. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Suzuki in view of Kahle to be used in a network processor to be keep costs low while providing a high level of network processing performance.

Response to Arguments

18. Applicant's arguments with respect to claims 1 and 4-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
19 December 2005

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